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Docket No.: CDST-C130.CIP

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Lee et al.

Serial No.: 09/588,115 Group Art Unit: 1765

Filed: May 31, 2000 Examiner: Not yet assigned.

Title: MULTILAYER ELECTRODE STRUCTURE AND METHOD FOR FORMING MULTILAYER ELECTRODE STRUCTURE FOR A FLAT PANEL DISPLAY DEVICE

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
S.R.	A	5,821,622	10/13/98	Tsuji et al.	257	763	4/17/96
S.R.	B	4,697,123	9/29/87	Shinoda et al.	315	169.4	11/9/81
S.R.	C	3,803,443	4/9/74	Hant	315	11	8/18/72
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Foreign Patent or Published Foreign Patent Application

Examiner Initial		Document No.	Publication Date	Country or Patent Office		Sub-	Translation	
S.R.	J	EP 503638 A2	9/16/92	EPO	H01J	1/30	X	
S.R.	K	EP 542271 A2	5/19/93	EPO	H01L	29/784	X	
S.R.	L	WO 98/43268	10/1/98	PCT	H01J	9/02	X	
S.R.	M	EP 964423 A1	12/15/99	EPO	H01J	31/12	X	
S.R.	N	EP 855451 A1	7/29/98	EPO	C23C	14/14	X	
S.R.	O	EP 731507 A1	9/11/96	EPO	H01L	29/49	X	
S.R.	P	DE 3720298 A1	12/29/88	DE	H01L	27/01		X
S.R.	Q	WO 98/49705	11/5/98	PCT	H01J	5/00	X	
S.R.	R	WO 93/21650	10/28/93	PCT	H01J	29/70	X	

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
S.R.	S	Patent Abstracts of Japan Vol. 017, no. 518 (E-1434), 17 September 1993 (1993-09-17) & JP 05 136411 A (Casio Comput Co Ltd), 1 June 1993 (1993-06-01) abstract
S.R.	T	Patent Abstracts of Japan Vol. 011, no. 003 (C-395), 7 January 1987 (1987-01-07) & JP 61 183433 A (Matsushita Electric Ind Co Ltd), 16 August 1986 (1986-08-16) abstract
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Examiner: Sikha Roy Date Considered: 3/4/02

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Attorney Docket No.: CDST-C130.1P

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Lee

Serial No.: 09/588,115 Group Art Unit: 2879

Filed: 5/31/00 Examiner: Not yet assigned

Title: MULTILAYER ELECTRODE STRUCTURE AND METHOD FOR FORMING MULTILAYER ELECTRODE STRUCTURE FOR A FLAT PANEL DISPLAY DEVICE

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
S.R.	A	5,601,466	2/11/97	Shen et al.	445	24	4/19/95
S.R.	B	6,019,657	2/1/00	Chakvorty et al.	445	24	10/29/98
S.R.	C	6,106,352	8/22/00	Fujii	445	24	3/17/99
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Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	J							
	K							
	L							
	M							
	N							
	O							
	P							
	Q							
	R							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
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Examiner: Sikhar Roy Date Considered: 3/4/02

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.